

## “DFT” for CAD Layout

*The following “Design for Test” (DFT) guidelines are provided to help insure that a bed-of-nails test fixture can be fabricated to test a PCB without sacrificing test coverage. This covers test point size and spacing as well as many other considerations.*

*In some instances not all test requirements can be met. Please feel free to contact Test Coach with any comments or questions on these guidelines.*

Thanks,

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### Test Point Definition

The term test point will be used to refer to any feature that is probed during an electrical test, i.e. test via, test pad, or through-hole lead. Test points can be utilized by all test processes including ICT, Flying Probe Testing, and Boundary Scan.

- A test via is a plated through-hole with an exposed annular ring; the test probe strikes either the solder that fills via holes during processing or the outer edges of the empty via barrel.
- A test pad is a solid area of exposed metallization in which there is no through-hole, and therefore the test probe strikes the flat surface of the feature.

All test points should be identified properly and associated with a net in the PCB’s CAD database and possibly on the Schematic as well. If a surface pad is placed and connected with a trace to a component pin, but not logically connected in the PCB database, it may be missed and not assigned a test probe in the test fixture.

Note: These guidelines will commonly refer to top and bottom of the PCB. On many products the bottom side of the PCB is the side probed. Although there are many exceptions to this rule, these notes will assume the bottom of the board is the side probed unless otherwise noted.

### Tooling Hole Requirement

The test probes in a test fixture are aligned to the PCB by the tooling pins.

- Place a minimum of two holes in opposite corners of the board.
- Tooling holes should be non-plated.
- Tooling hole size tolerance of +0.002" / -0.001".
- Tooling holes should be placed asymmetrically to prevent the test operator from placing the PCB on the fixture backwards and damaging the test equipment.
- Tooling pins should be made of a hardened material so they break before they bend and cause contact problems.
- Install 4 caging pins around the PCB so that the board cannot jump off the tooling pins during activation of the fixture and to prevent partial insertion on tooling pins. The edge of the cage pin should be placed less than ½ the diameter of the smallest tooling pin from the edge of the board. The PCB will be guided onto the tooling pins if they are tapered at the top.

**Accessibility**

A minimum of one test point per signal net is required on the bottom of the board. The number of test points required, per net type, shall be calculated using the following criteria:

Signal Net	1
Power Net	2 + (# connections on that net)/20; 8 maximum
Ground Net	10 + (# connections on that net)/20; no maximum *
Isolated Power/Ground Net	2
Low Value Critical passives	2 on each side of component for 4-wire measurements
Unused Pins on SMT Connectors	1
Unused Pins on ICs/BGAs	1 (Tie off unused inputs and put test points on outputs if shorts can degrade the life of the parts.)

\* Multiple ground test points dramatically reduce noise, improve signal integrity, and produce better repeatability. Especially in complex digital testing and boundary scan.

**Priority of Test Targets:**

1. Test Via
2. Test Pad
3. Through-hole Lead (see following section)

Priority of pads or vias is highly process-related and should be discussed with your test department. For example, probing IR reflowed OSP boards is commonly done successfully. However, the combination of IR reflowed OSP boards also placed through a solder wave may create problems when attempting to probe Test Pads, but not Test Vias. (For more information contact Test Coach)

**Special note on Microvia boards:** Test probes with enough force and an edge to reliably contact test pads on standard multi-layer boards may penetrate through the test pads and short out to internal layers on Microvia boards due to the lack of fiberglass in the insulated layers. Test Vias provide a stronger target in this situation.

**Through-hole Component Leads as Test Points**

- If you choose to use through-hole component leads over test pads or vias, the leads of the through-hole component should be reviewed to ensure repeatable contact can be made by the test probe. It is important that when a through-hole lead is used as a test point, the lead protrusion must be of a consistent length and strong enough to withstand the compressive force of the test probe. Components with soft legs that will deflect the ICT probe should not be used as test points because they will produce false shorts. Examples of those components are certain transformers and LED's.
- Through-hole components that are stuffed on one version of a common board, but not another, should not be used as a test point location. Different probe styles are required to hit leads or empty holes. Through-hole leads with a drill size of 0.060" or greater should not be used as test points.

- Do not use Pin and Paste through-hole component leads as test points. These leads build up a great amount of flux, which will create contact problems with test probes. Test points in the form of pads or vias are required to be added and can then be distributed throughout the PCB.
- Through-hole connector pins on a grid of 0.069" or less will need to have test points for alternating pin locations placed elsewhere on the board to achieve proper test point to test point spacing for the connector. Restated, it is undesirable to use 50mil test probes on through-hole components. This will also be required for the unused pins on these connectors for shorts testing.

Contact your test department to determine whether or not through-hole components used in your application are acceptable.

### Test Via drill size

The drill hole size of test vias has a significant impact on test probe contact repeatability. It is intended for the test probe to strike either the solder that fills the via hole during processing or the outer edge of the empty via barrel. If the via drill size is too large, the test probe may enter the hole and hit contaminates before it makes contact with the outside ridge of the via barrel. Typically a 0.012" drill is acceptable with 100, 75, and 50 mil test probes. Using larger drill sizes may eliminate the use of some of the smaller diameter test probes.

### SMD Connector Pads as Test Points

SMD connector pads are commonly used as test points one of two ways: as gold fingers, or as unpopulated debug headers. The customer must understand that that if SMD connector pads are used as test points, the test probe may leave an impression in the pad after contact is made.

Normal test point spacing rules apply to SMD connector pads. If the pads are rectangular in shape, test probes may be staggered to the top and bottom of the pad to obtain larger test point spacing.

### Distribution

Test points should be evenly distributed across the bottom side of the PCB. When the probes are concentrated in one area, you create an area of high stress on the board. If the concentration is under a BGA, it may not be possible to apply enough counter force from the opposite side with push fingers. To avoid potential damage to your board, upfront efforts should be made to distribute your test points.

### Test Point Size in Order of Preference

<u>Priority</u>	<u>Target Size</u>	<u>Comments</u>
1	0.035"	Provides most ideal target size relative to tolerance build up of PCB and test fixture
2	0.030"	Provides an acceptable target size when proper tooling holes are available.
3	< 0.030"	Test fixture may require a probe guide increasing overall cost. Contact repeatability may be sacrificed as well.

**Test Point Spacing on the Bottom Side of the PCB**

## Center to Center Spacing

<u>Priority</u>	<u>Preferred</u>	<u>Acceptable</u>	<u>Comments</u>
1	0.100"	0.085"	Will allow the use of adjacent 100 mil test probes.
2	0.084"	0.070"	Will allow the use of adjacent 75 mil test probes.
3	0.069"	0.050"	Will allow the use of adjacent 50 mil test probes.
4 *	0.049"	0.035"	* <b>Consult your test department.</b>

Ideally, the largest test pads used along with 100mil test probes provides the most repeatable and cost effective solution. In practice, 0.035" bottom side test pads with 0.070" minimum center to center spacing are used successfully and are considered a standard by many. Smaller sized test pads at 0.050" center-to-center are also commonly used, but with some repeatability sacrifices, higher fixture fabrication and maintenance costs.

**Test Point to Feature Clearance**

- Test Point to **Tooling hole**: clearance of 0.125". (Clearance indicated refers to annular ring).
- Test Point to a **TALL component greater than 0.100" height**: clearance of 0.065". (Clearance indicated is measured from the edge of the test target to the edge of adjacent component.) **NOTE 1**
- Test Point to a **short component less than 0.100" in height**: clearance of 0.040". (Clearance indicated is measured from the edge of the test target to the edge of adjacent component.) **NOTE 1**
- Test points to a **component/IC that will be tested with vectorless testing sensor plates (TestJet)**: a minimum distance of 0.250". This holds true for both top and bottom side components.
- Test Via or Pad to a **Through-hole test point**: clearance of 0.065". This helps insure a 75mil or 100mil probe on your through hole lead.
- Test Point to **routing via**: clearance of 0.025".
- Test Point to **PCB edge**: clearance of 0.125".
- Test Point to **Silk Screen Text**: clearance of 0.015".
- Test Via or PAD to **edge of selective wave window**: clearance of 0.200"
- Test Via or PAD to **trace**: clearance of 0.010".
- Test Point to **Gold Finders**: clearance of 0.200". **NOTE 2**

**NOTE 1:** Consider the worst case placement of components when determining a parts outline to prevent probe damage. IPC and other specs state that a component can be placed a percentage off its pads and still be acceptable.

**NOTE 2:** Clearance required from test point to gold or carbon fingers may vary depending on the method used to prevent solder build up. The measurement shall be taken from the inner most edge of the gold finger to edge of the test point.

- If the gold fingers are shielded using protectors mounted on the wave solder machine the clearance must be 0.200".
- If the gold fingers are protected using Kapton tape the clearance must be 0.200".
- If carbon fingers are present maintain a clearance of 0.050". This is due to the fact that solder does not adhere to carbon fingers.

**Assure Clearance Space for Push Fingers on the Top Side of the PCB**

In order to minimize board flex and provide even pressure against test probes, push fingers are required to be on the top plate of the fixture. These fingers will contact the surface of the PCB and ensure the PCB remains flat during testing by providing a counter force to the bottom side test probes. Maintain the following keep-out and spacing criteria:

- Disperse a 1.50"-2.00" square keep-out grid evenly across the surface of the PWB.
- Maintain a 0.160" diameter component keep out in the area of each push finger.
- Additional sites may be required in areas of high probe density.
- Odd shaped boards (L shaped), those with cut-outs, or notches may require additional push finger sites.

**Spacing on the Top Side of the PCB**

If it is impossible to obtain access to every net on the bottom side of the PCB, and after all limited access testing techniques and DFT considerations have been exhausted, access from the top side can be carefully considered. It must be understood that the cost of the test fixture increases greatly due to the addition of a top side probe plate along with transferring of the tester's resources from the bottom side to the top.

Test points for critical nets such as: clocks, those used for in-line programming, memory control pins, boundary scan ports, serial data, clocklines, etc., should NOT be placed on the top side of the PCB.

- Test Pad Size of 0.35" at a spacing of 0.070" should be maintained with proper tooling holes for acceptable contact repeatability.

In practice, top side test points with 0.050" center-to-center have also been used, but with some repeatability sacrifices over time along with higher fixture fabrication and maintenance costs.

Also, remember to have some protection for the top side test probes in the fixture so they are not accidentally damaged when the operator removes and inserts boards into the fixture.

**DFT Rules for Revising an Artwork**

Modification of a bed-of-nails test fixture is possible when the CAD changes. The following rules should be used to minimize the cost and time it takes to modify an existing fixture:

- Do not move tooling pin holes.
- Do not move test points unless absolutely necessary.
- Do not put a new test point within 0.100" from an old test point that is being removed or an existing test point.
- Do not rename existing components.
- Do not name new components the same name as components that have been removed.
- If a connection on a net has changed, rename the net.
- If a net splits into two or more nets do not re-use the old net name, create two or more new names.
- Keep the diameter of new test points at 0.035" to ensure a reliable contact. When fixture vendors re-drill holes for probe sockets into an existing fixture, they may not be as accurate as when the original fixture was fabricated.

**Panelization Consideration**

To reduce handling and test time, boards are often tested as a panel. In many situations, the individual boards of the panel can be tested in parallel. The following can help ensure this can be accomplished:

- Ensure tooling holes are on the PCB and not on the break-away panel material.
- If a panel is symmetrical, it may be difficult to match the test data to the board position. Ensure the panel is keyed to prevent improper placement on the fixture.
- Provide spacing between boards to accommodate overhanging components.